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| **KLS Gogte Institute of Technology**  **Department of Computer Science and Engineering**  **IA- III**  **Subject : Logic Design and ApplicationsCode : 15CS32 Semester : IIIDivision : A,B,C Date:11/11/2016 Time:1pm-2pm Max.Marks:25** |
| **Note: i) Answer all questions.**  **ii) All questions carry*five* marks**   1. Design a MOD 4 synchronous counter using JK flip flop and draw the logic diagram for the same.   **[L6,CLO 3,PO 1,2]**   1. Explain 3-bit ripple (asynchronous) UP counter with neat diagram and waveform.   [**L3, CLO 3,PO 1,2,3]**   1. Illustrate IC 7490 as MOD 10 counter and modify the circuit for MOD 8 counter.   **[L3, CLO 3, PO 1,2]**   1. Explain the working of 4 bit twisted ring counter (Johnson counter) with neat timing diagram.   **[L3, CLO 3,PO 1,2]**   1. Write the HDL Verilog code for following circuits in data flow model. 2. Y= ABC+AC+ABC 3. 4:1 MULTIPLEXER**[L3,CLO 3,PO 1,2,3]** |